The following is a complete listing of all claims in the application, with an indication of the status of each:

Listing of claims:

1	1. (Previously Presented) An instruction buffer comprising:
2	a sequence of instructions arranged in an order determined beforehand;
3	and
4	a first buffer including entries arranged in a preselected entry number
5	order for storing said sequence of instructions; and
6	a second buffer including other entries for storing instructions, wherein
7	an instruction stored in any one of said other entries earlier than other
8	instructions is issued earlier than said other instructions,
9	wherein any one instruction of said sequence of instructions stored in
10	any one of the entries designated by a low relatively lower entry number is
11	prior, in order, to another instruction stored in another entry designated by a
12	high relatively higher entry number.
2	
1	2. (Original) The instruction buffer as claimed in claim 1, wherein the entries
2	each show whether or not the instruction stored therein is ready to be issued.
1	3. (Previously Presented) The instruction buffer as claimed in claim 2,
2	wherein the instruction is first issued from among the entries whose
3	instructions are ready to be issued is the entry having a lowest entry number
4	among said entries whose instructions are ready to be issued.

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1	4. (Original) The instruction buffer as claimed in claim 3, wherein the entries
2	storing the instructions are lower in entry number than the entries storing no
3	instructions.
1	5. (Cancelled)
1	6. (Previously Presented) A method of controlling a buffer queue, comprising
2	the steps of:
3	generating a first group of instructions in an a priority order
4	determined beforehand;
5	generating a second group of instructions belonging to said first group
6	of instructions and capable of being executed; and
7	executing one instruction of said second group of instructions highest
8	in priority order.
1	7. (Previously Presented) The method as claimed in claim 6, further
2	comprising the steps of:
3	generating a third group of instructions included in said first group of
4	instructions; and
5	generating a fourth group of instructions included in said first group of
6	instructions and not dependent on said third group of instructions;
7	wherein when one of said fourth group of instructions highest in
8	priority order does not belong to said second group of instructions, none no
9	instruction of said fourth group of instructions is executed.

I	8. (Previously Presented) The method as claimed in claim 7, wherein one of
2	preselected two instructions belonging to said third group or fourth group of
3	instructions is not executable until the other instruction of said two
4	instructions is executed.
1	9. (Original) The method as claimed in claim 8, wherein the instructions
2	belonging to said third group are executed at the same time as the instructions
3	belonging to said fourth group.
1	10. (Original) The method as claimed in claim 9, wherein the instructions
2	belonging to said third group and the instructions belonging to said fourth
3	group and operation instructions and memory access instructions, respectively
1	11 (New). A buffer queue control comprising:
2	a reorder buffer for subsequently registering a plurality of instructions
3	in an order of instruction:
4	a first buffer for storing first instructions included in the plurality of
5	instructions;
6	a second buffer for storing, among the plurality of instructions, second
7	instruction other than the first instructions;
8	said second instructions including an instruction that should be issued
9	after first instruction;
10	said first buffer including a plurality of first entries for sequentially
11	storing the first instructions in said order of instruction;
12	said buffer queue control further comprising the steps of:
13	releasing any one of the plurality of first entries that stores an
14	instruction issued;

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15	shifting any one of the first instructions that is not issued to an entry
16	prior, in order, by one;
17	issuing one of the second instructions, which can be issued, earliest in
18	said order of instruction; and
19	deleting any one of the plurality of instructions that has been executed
20	and is earlier, in said order of instruction, than instruction not executed.
1	12 (New). The buffer queue control as claimed in claim 11 further comprising
2	the step of issuing any one of the first instructions that is earliest in said order
3	of instruction and ready to be issued.
1	13 (New). The buffer queue control as claimed in claim 12, wherein said
2	second buffer comprises a plurality of second entries each for storing a
3	particular one of the second instructions in said order of instruction, an
4	issuance pointer for controlling issuance of said second instructions, and a
5	head pointer indicative of an entry that has been issued last.
1	14 (New). The buffer queue control as claimed in claim 13, wherein one of
2	first instructions can be executed at the same time as one of second
3	instructions.
1	15 (New). The buffer queue control as claimed in claim 14, wherein the first
2	instructions comprise operation instructions while the second instructions
3	comprise memory access instructions.